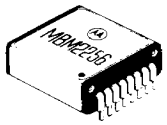
MOTOROLA

MBM2256

Advance Information

256 K x 1-BIT MAGNETIC BUBBLE MEMORY DEVICE



GENERAL DESCRIPTION

The MBM2256 is a 262,144 (2^{18}) bit magnetic bubble memory device. All required magnetic components including the permanent magnets, the drive field coils and protective magnetic shield are integral parts of the device. The package is a 1.15 x 1.1 x 0.36 inch 16-pin DIP.

The MBM2256 features a dual block-replicate organization with swap gates on the input track. Data storage is organized as 256 storage loops of 1024-bits each. Additional loops are provided to store the error correction code and as redundant loops. In one of two dedicated map loops on-chip the redundant map loop data is stored.

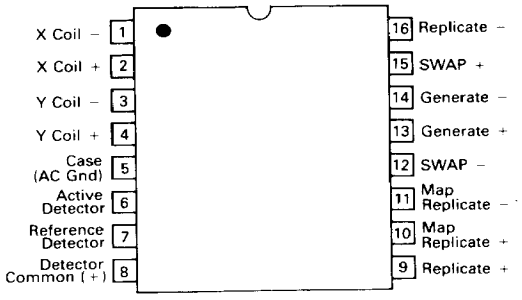
The MBM2256 can be operated synchronously or asynchronously. Average access time to a page of data is less than 7.0 ms at 100 kHz. Data transfer rate is 125 kilobits per second at 125 kHz. Average power dissipation at 125 kHz is 0.8 Watts. The device will operate over a case temperature range of 0°C to 70°C, and data is retained without power from −40°C to 100°C.

The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements ensures excellent conductivity while greatly increasing resistance to problems associated with electromigration.

FEATURES

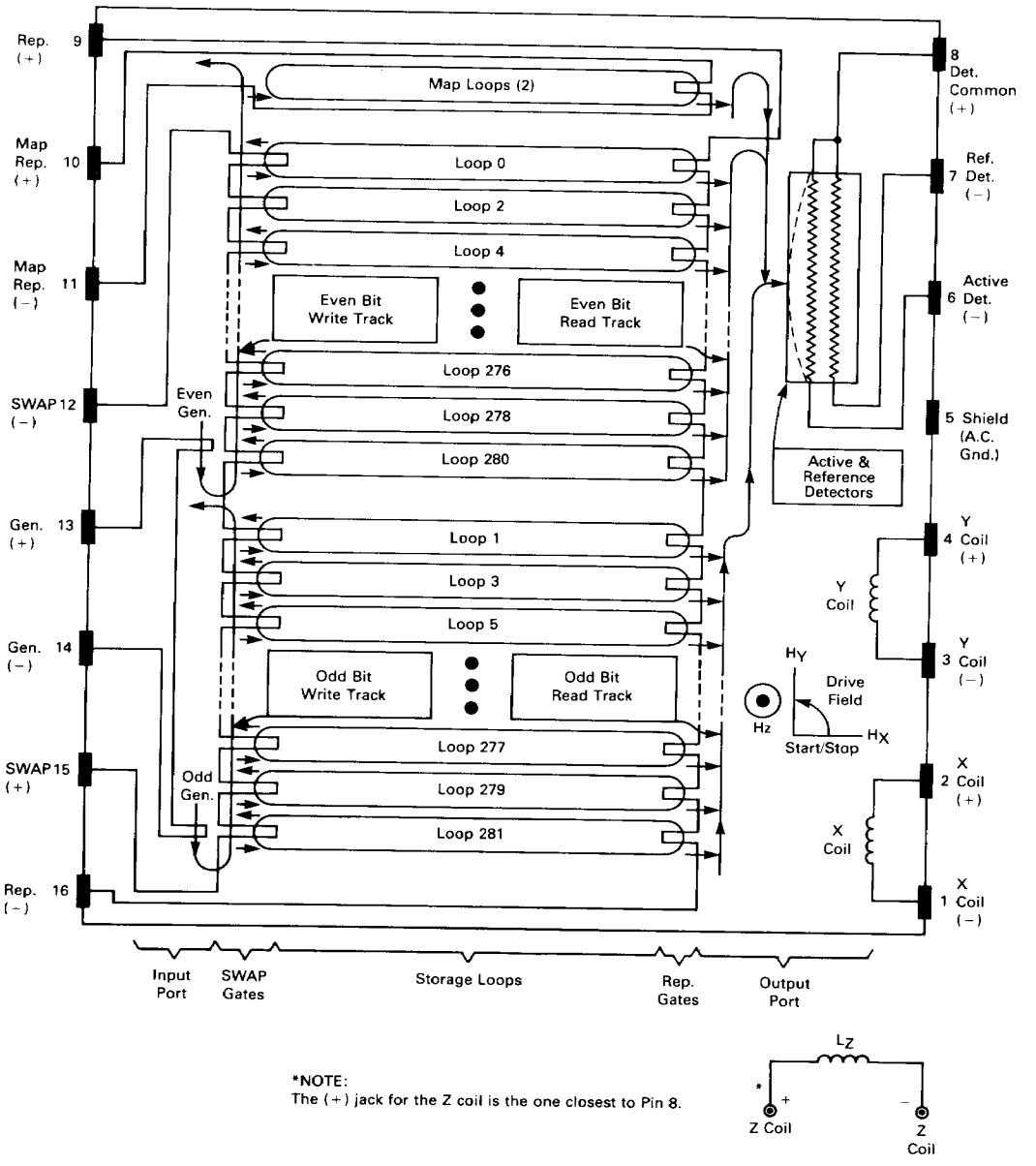
- Non-volatile
- High Density
- Solid State
- Low Power
- Start/Stop Capability
- Page-Oriented Access
- On-Chip Redundant Loop Map
- Swap Gates
- Block Replicate
- Error Correction Code Storage
- 16-Pin Dual-in-Line Package

Pin Assignment



This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 — BLOCK DIAGRAM



*NOTE:
The (+) jack for the Z coil is the one closest to Pin 8.

ABSOLUTE MAXIMUM RATINGS

Rating	Min	Max	Unit
Operating Temperature (Case) (T_C)	0	70	°C
Non-Volatile Storage Temperature	−40	100	°C
Storage Temperature	−40	120	°C
External Magnetic Field	—	20	Oe
Peak Current In X Coil*	—	900	mA
Peak Current In Y Coil*	—	1,100	mA
Peak Current In Z Coil*	—	3,000	mAdc
Peak Replicate Current	—	40	mAdc
Peak Generate Current	—	40	mAdc
Peak Swap Current	—	30	mAdc
Peak Detector Current	—	6.0	mAdc
Maximum Coil Disturb Current With Data Retention	—	10	mA
Maximum Pin To Pin Voltage	—	55	Volts

*These peak currents are allowed subject to the device temperature not exceeding the temperature limits.

ELECTRICAL CHARACTERISTICS (T_C = 0°C to 70°C, rotating field frequency (f_o) = 125 kHz unless otherwise noted).

FUNCTION CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Generate Current	I_G	180	—	220	mA
Swap Current	I_S	25	—	31	mA
Replicate Cut Current	I_{RC}	75	—	95	mA
Replicate Transfer Current	I_{RT}	28	—	42	mA
Map Replicate Cut Current	I_{RCM}	75	—	95	mA
Map Replicate Transfer Current	I_{RTM}	28	—	42	mA
Map Transfer In Current	I_{TM}	−24	—	−30	mA
Detector Current	I_{DA}, I_{DR}	—	5.0	5.8	mA

X,Y COIL DRIVE (See Figure 2.)

Parameter	Symbol	Min	Typ	Max	Unit
Coil Driver Supply Voltage	V_x, V_y	11.4	12	12.6	V
Coil Driver Switch On Resistance (2 Switches In Series)	R_{on}	0.7	—	1.8	Ohms
Coil Driver Clamp Diode Drop (2 Diodes In Series)	V_{clamp}	—	—	1.6	V
X Coil Peak Current (L_x = nom, V_x = nom, R_{on}, V_{clamp} = nom)	I_{XP}	—	630	—	mA
Y Coil Peak Current (L_y = nom, V_y = nom) (R_{on}, V_{clamp} = nom)	I_{YP}	—	770	—	mA
Coil Current Offset	I_{xo}, I_{yo}	−10	—	+10	mA
Stop Current Overshoot	I_{so}	—	—	+10 −0	mA
Total Coil Power	P_c	—	—	1.0	W

Z COIL DRIVE

Z Coil Sensitivity		—	26.5	—	Oe A
Z Coil Current Simultaneously Erase All Data Stored	I_{zap}				A
(Rotating Field On)		2.0	—	—	
(Rotating Field Off)		3.0	—	—	
Duration of Erase Current	t_{ZAP}	0.5	—	10	ms

Bubble

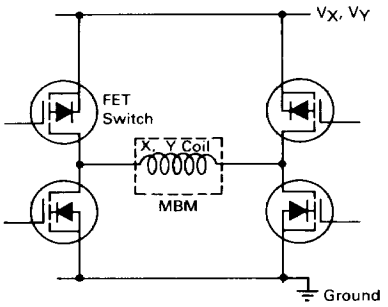
SCOPE

This specification describes the magnetic, electrical, mechanical and environmental parameters of the 256K bit magnetic bubble device, MBM2256, as manufactured by Motorola Inc.

DEVICE ORGANIZATION

The 256K bit bubble memory chip uses a block-replicate organization with true swap gates on the input track. The storage area is arranged as 256 storage loops each with 1,024 bit locations. Additional loops are provided for error correction (6) and defect tolerance (20) giving a total of 282 loops. Data is written and read at the clock frequency which is the rotating field frequency. Figure 1 is a schematic diagram of the 256K bit chip.

FIGURE 2 — X, Y COIL DRIVE



(a.) TYPICAL DRIVE CIRCUIT

Data Input

The device is organized into two halves — odd and even. To write into the device the same data pattern is written simultaneously into both the odd and even input tracks. Due to the spacing between minor loops only alternate bits can be aligned with adjacent minor loops. An extra bit propagation delay on the odd input track causes odd bits to align with odd loops and even bits with even loops such that the correct bit is written into each loop. The swap gate automatically clears the old data as new data is written into the loops.

Data Output

To read the data, one bit is replicated from each minor loop into the output track, again arranged as an odd and even half. The alternate bit data streams are then interleaved prior to entering the detector. The data is therefore written in and read out of the bubble device at the clock frequency although the data does divide and recombine within the chip.

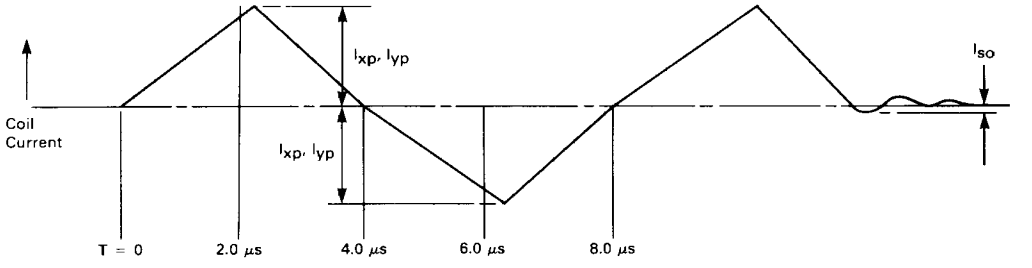
Redundancy

Of the 282 storage loops 256 are allocated for data, 6 for error correction and 20 for redundancy. These 20 loops are used to mask inoperable minor loops and improve performance. Twenty loops are always declared redundant. Data should not be written into the redundant loops.

Redundancy Map

In addition to the 282 storage loops the chip contains two map loops. These loops have their own transfer-in and replicate gates but share the generator and detector with the storage loops. Only one loop is required and is chosen at final test. The chosen loop is used to store the data which identifies the redundant loop map. A "one" designates a usable loop; a "zero" a non-usable loop. Preceding this map code is a stream of 64 "zeros" followed by a "one" and a "zero" which may be used to synchronize the external control circuitry with the memory. The map loop used for storage of the redundancy information is also identified in the code (see Coding of Redundancy Map). Since only alternate bit positions are written into the map loop to enhance reliability, intervening bits are always zero and are ignored during read (see Map Read Operation paragraph).

The redundancy map is also printed on the label of each device using hexadecimal format. Two digits are used per loop. Instead of providing the absolute loop number, the incremental difference between non-usable loops is printed. For example, if the first bad loop is #7, and the next two are 19 and 23, the sequence



(b.) TYPICAL RISE/FALL IMBALANCE DUE TO DRIVE CIRCUIT

070C04 will be printed on the label. This format allows for an incremental difference between two non-usable loops of up to 255 (FF).

Coding of Redundancy Map (The map loop contains 512 bits of information in five fields.)

Pattern	Field	Number of Bits	Note
MM---MM	Map Data	282	(1)
EE---EE	Error Correction	12	(2)
LL	Loop	2	(3)
UU---UU	User	150	(4)
00---0010	Sync	66	(5)

NOTE:
(1) Each bit corresponds to a data loop in sequence
M = 1 identifies a usable loop (262).
M = 0 identifies a redundant loop (20).
(2) Error correction code used is a fire code applied only to the map data.
(3) Identifies which map loop contains the redundancy information
01 — loop #1, 10 — loop #2.
(4) This field may contain factory-pertinent information. It will not contain a duplicate of the sync pattern.
(5) The sync pattern is used to locate the beginning of the map data field and identifies data page zero.

Organizational Specifications

Bits/Loop	1,024
Total Data Loops	282
Usable Data Loops	262
Error Correction Loops	6
User Data Loops	256
Total User Storage	262,144 Bits
Map Loops	2

FUNCTIONAL DESCRIPTION

Write Data Operation

Writing data is accomplished by generating the new data with a series of pulses applied to pins 13 and 14, starting t_{PGSF} before the swap operation. As the device continues to cycle after all data is generated, the new data and the old will be aligned at the swap gates after t_{PGSL}. A swap pulse is applied to pins 12 and 15 at this time, swapping the new data in and the old data out. Unused bits from the even and odd sides along with the old data are propagated out and discarded beyond the active area.

Read Data Operation

To read data, the device must be cycled until the desired page is aligned with the replicate gates on the output side of the storage loops. A replicate cut pulse is applied to pins 9 and 16 to duplicate the page. This is immediately followed by a replicate transfer pulse which causes the duplicate bubbles to propagate into alternate positions on the two output tracks.

Propagation along the output tracks occurs during t_{PRD}. During this time, the odd and even output bits are merged.

Detection occurs when a bubble passes under the magnetoresistive detector element. The bubble's magnetic field causes the detector element to change resistance. By passing a constant current through the detector, this is converted to a voltage signal. A dummy detector which is not influenced by magnetic bubbles is used to cancel the background magnetoresistive signal.

Output bubbles are discarded beyond the active area after detection. A complete page is read in t_{PRDL}.

INTERFACE IMPEDANCES

Parameter	Symbol	Min	Typ	Max	Unit
Generate (1)	r_G	4.5	—	18	Ω
Swap (1)	r_S	180	—	540	Ω
Replicate (1)	r_R	130	—	320	Ω
Map Replicate (1) (Includes Map Transfer-In)	r_M	18	—	56	Ω
Detector (Active and Reference) (1)	r_{DS}, r_{DR}	950	—	2000	Ω
Detector Active/Reference Ratio	—	0.985	—	1.015	—
X Coil Inductance	L_x	34	—	37	μH
Y Coil Inductance	L_y	27	—	30	μH
Z Coil Inductance	L_z	25	—	35	μH
X Coil dc Resistance Non-operating, 25°C	r_x dc	—	2.7	—	Ω
Y Coil dc Resistance Non-operating, 25°C	r_y dc	—	1.1	—	Ω
Z Coil dc Resistance Non-operating, 25°C	r_z dc	—	0.75	—	Ω
X Coil ac Resistance (1)	r_x ac	2.5	—	4.0	Ω
Y Coil ac Resistance (1)	r_y ac	1.5	—	2.5	Ω

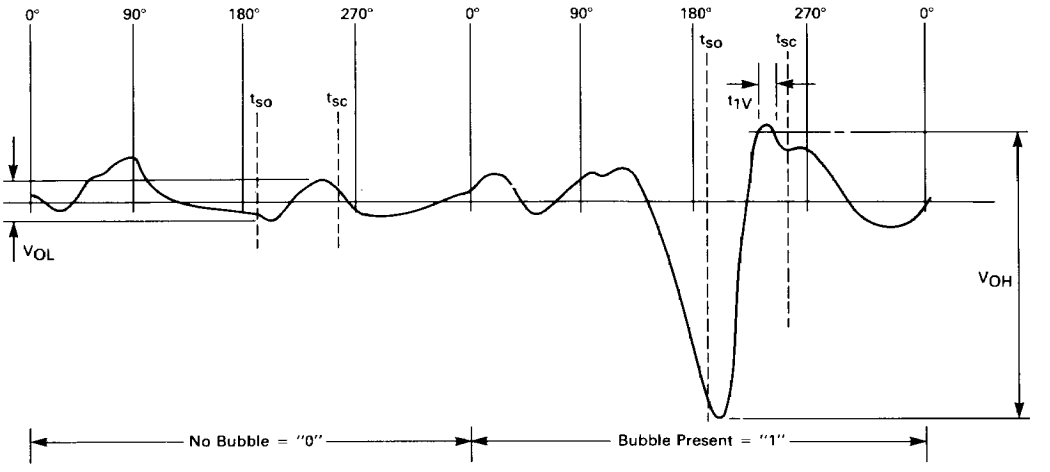
NOTE:
(1) Minimum value is at T_C = 0°C, device non-operating, maximum value is at T_C = 70°C, device operating.

OUTPUT SIGNALS (T_C = 0°C to 70°C, f_o = 125 kHz)

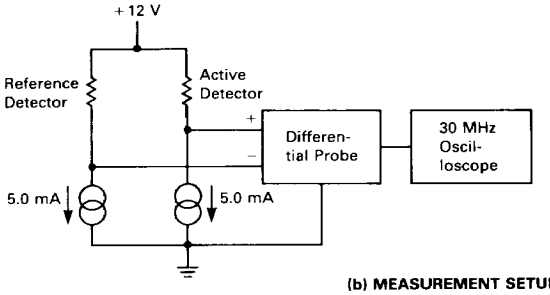
Parameter	Symbol	Min	Typ	Max	Unit
Common-Mode Output Signal (I_{DA} = I_{DR} = 5.0 mA) Differential Peak-to-Peak Output Voltage (1) (I_d = 5.0 mA. See Figure 1 for measurement details.)	V_{cm}	—	—	50	mV
Logic 1 (Bubble Present)	V_{OH}	TBD	—	—	mV
Logic 0 (No Bubble)	V_{OL}	—	—	TBD	mV
Signal Strobe Leading Edge Phase	t_{so}	—	191	—	Degrees
Signal Strobe Trailing Edge Phase	t_{sc}	—	258	—	Degrees
Logic 1 Valid Window	t_{1V}	50	—	—	ns

NOTE:
(1) V_{OH} is defined as the difference between the most negative and the most positive signal excursions which occur within the phase window t_{so} to t_{sc} when a bubble is being detected. V_{OL} is similarly defined for the case of no bubble being detected. See Figure 3.

FIGURE 3 —



(a) DETECTOR BRIDGE OUTPUT



Scope Input Impedance:
≥ 2M
≤ 5.0 pF

Common-Mode Rejection:
≥ 60 dB

Frequency Response:
≥ 5.0 MHz

(b) MEASUREMENT SETUP

Bubble

Map Read Operation

To read the contents of the map, a series of alternate cycle replicate pulses, identical to data replicate pulses, is applied to pins 10 and 11. Data will be available after t_{PMRD}. Since map data is only loaded into alternate positions in the loop, one pass may result in no data. This procedure is then repeated after delaying one cycle. The outputs from the two map loops are merged, but only one loop contains data. See "Coding of Redundancy Map Loops" for decoding information.

Map Write Operation

Writing the map loop is accomplished by generating map information as normal data on alternate cycles. After t_{PGT1} or t_{PGT2}, pins 10 and 11 are pulsed with a series of negative map transfer pulses on alternate cycles. Selecting t_{PGT1} writes into map loop 1, selecting t_{PGT2} writes into map loop 2.

TIMING CHARACTERISTICS (T_C = 0°C, f_O = 125 kHz unless otherwise noted. See Figure 4 for test conditions).*

WRITE CYCLE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Generate First Bit to Swap In (1)	$t_{PGS(F)}$	—	294	—	Cycles
Generate Last Bit to Swap In (1)	$t_{PGS(L)}$	—	13	—	Cycles
Swap In to Replicate Out (1)	t_{PSR}	—	514	—	Cycles
Swap In to Non-Volatile Storage (2)	t_{PS}	—	2	—	Cycles
Generate Delay Time (3)	t_{DG}	70	—	120	Degrees
Generate Pulse Width (4)	t_{WG}	140	210	280	ns
Generate Fall Time (10%–90% of pk Amplitude)	t_{FG}	200	—	400	ns
Swap Delay Time (3)	t_{DS}	270	—	330	Degrees
Swap Pulse Width	t_{WS}	340	370	400	Degrees

READ CYCLE TIMING

Replicate Out to Detect First Bit (1)	$t_{PRD(F)}$	—	180	—	Cycles
Replicate Out to Detect Last Bit (1)	$t_{PRD(L)}$	—	461	—	Cycles
Replicate Out to Swap In (1)	t_{PRS}	—	510	—	Cycles
Replicate Delay Time (3)	t_{DR}	−10	—	20	Degrees
Replicate Cut Pulse Width	t_{WRC}	210	280	350	ns
Replicate Transfer Pulse Width	t_{WRT}	80	100	120	Degrees

MAP READ AND WRITE CYCLE TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Map Replicate to Detect	t_{PMRD}	—	188	—	Cycles
Generate to Map Loop #1 Transfer	T_{PGT1}	—	308	—	Cycles
Generate to Map Loop #2 Transfer	t_{PGT2}	—	305	—	Cycles
Map Loop Transfer-In to Replicate	t_{PTR}	—	516	—	Cycles
Map Replicate Delay Time (3)	t_{DRM}	−10	—	20	Degrees
Map Replicate Cut Pulse Width	t_{WRCM}	210	280	350	ns
Map Replicate Transfer Pulse Width	t_{WRTM}	80	100	120	Degrees
Map Transfer-In Delay Time	t_{DTM}	270	—	330	Degrees
Map Transfer-In Pulse Width	t_{WTM}	200	220	240	Degrees

NOTES:
* All pulses to have rise and fall times ≤ 80 ns (10%–90% of peak amplitude) unless otherwise noted.
(1) Propagation times are defined from the beginning of the cycle in which the first signal occurs to the beginning of the cycle in which the second signal occurs.
(2) Data is non-volatile at the end of the cycle in which the swap current is turned off.
(3) These parameter limits are guaranteed when the device is driven with the X and Y current shown in Figure 4. Deviations from these drive conditions may cause these limits to change in absolute angle, but the phase range (max–min) will remain as specified.
(4) Generate pulse width is defined from 50% amplitude on the rising edge to 90% amplitude on the falling edge.

FIGURE 4 — TEST CONDITIONS — X AND Y CURRENT WAVEFORMS

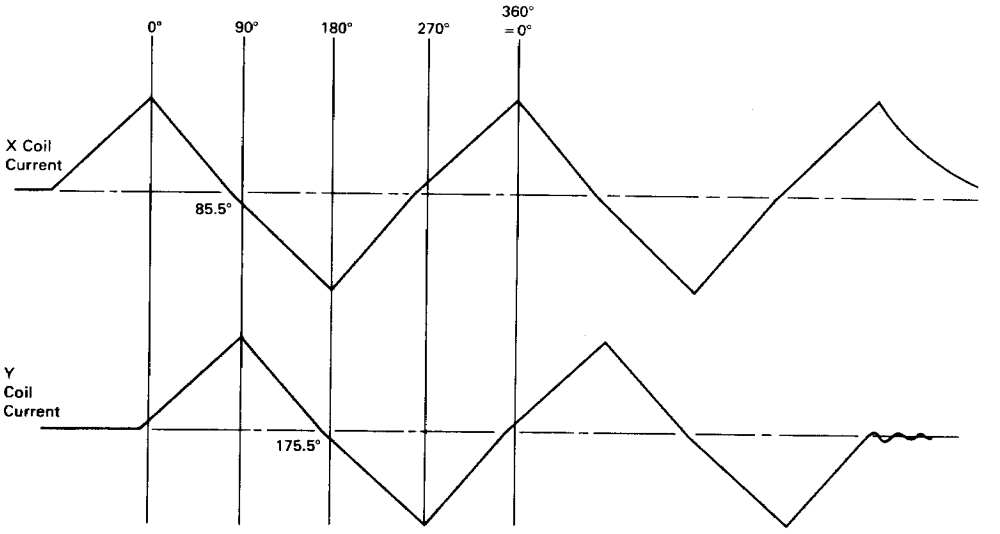
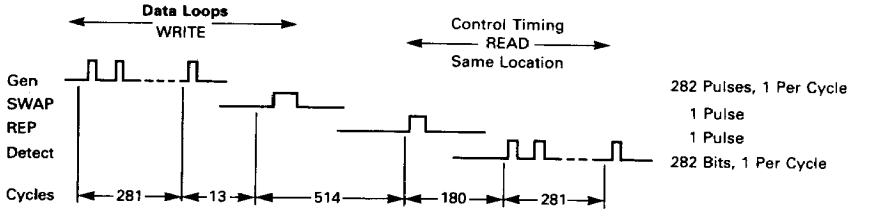
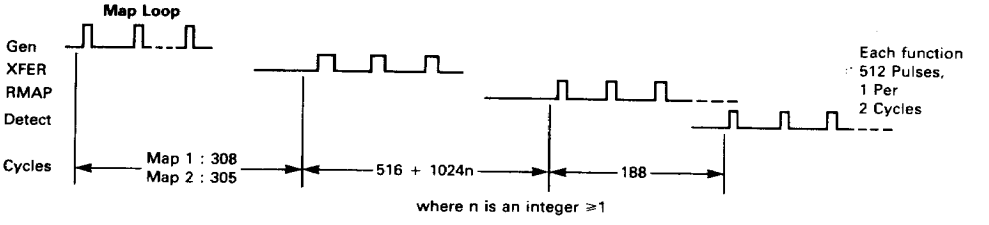


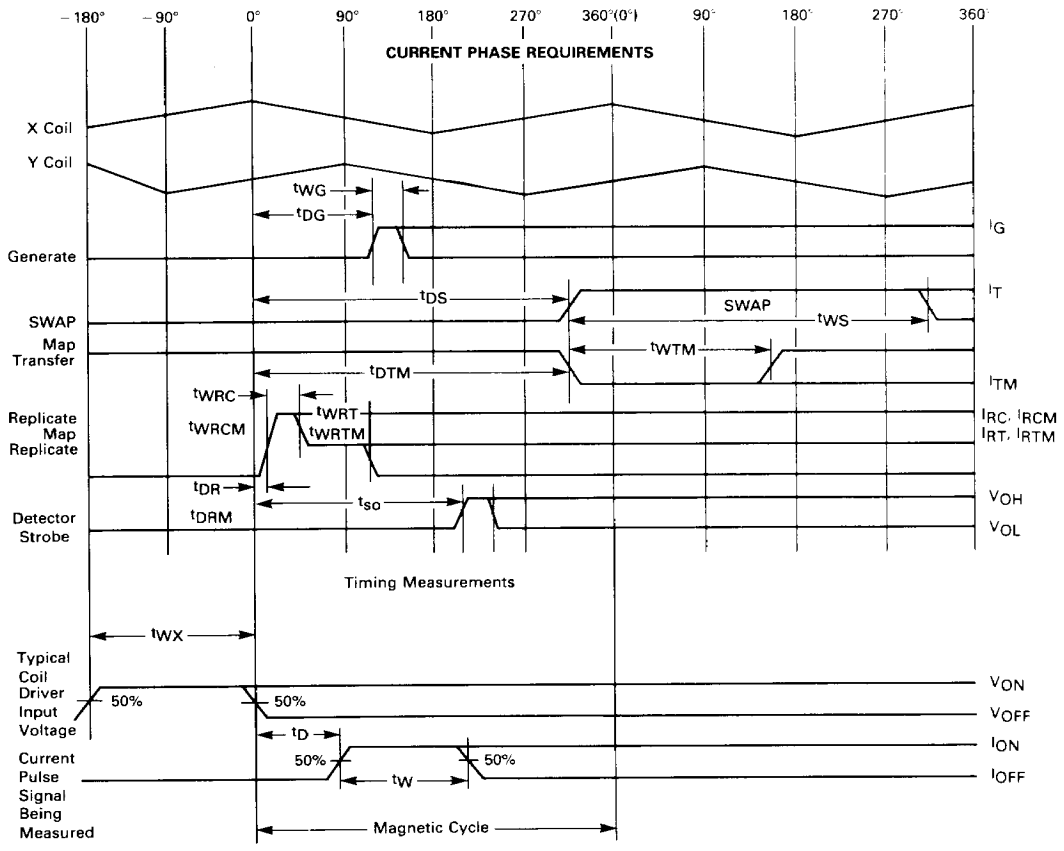
FIGURE 5





Bubble

FIGURE 6 — X, Y COIL TIMING



TIMING OF PULSES WITHIN A CYCLE

MECHANICAL SPECIFICATION

Package

The MBM2256 device is a 16-pin dual-in-line package. The die is mounted on a printed circuit board carrier attached to a beryllium copper leadframe and encapsulated in plastic compound. Two orthogonal coils and a pair of permanent magnets enclose the die and the whole device is molded into a Mumetal shield. A Z coil is included in the device to facilitate testing and extended temperature range operation.

Mechanical Data

Package Size	1.15 x 1.10 x 0.36 in (29.2 x 27.9 x 9.14) mm
Package Weight	28 gm.

Bubble

ENVIRONMENTAL SPECIFICATION

Temperature Ranges

Continuous operation at 125 kHz. Case temperature 0° to 70°C. Non-operating, non-volatile storage −40° to 100°C.

External Magnetic Fields

When subjected to an external magnetic field of 20 Oe maximum in any direction, the device will continue to operate satisfactorily as long as the parameters are kept within the range specified in this document.

Screen Tests	All Parts 100%
Die Visual	100X Inspection consistent with MIL-883B, Method 2010, Cond. B
Stabilization Bake	As per MIL-STD-883B, Method 1008, Condition C, 150°C for 24 hours
Temperature Cycling	As per MIL-STD-883B, Method 1010, Condition B, 10 cycles −55°C → 125°C
External Visual	MIL-883B, Method 2009

Qualification Testing

Bond Strength	MIL-883B, Method 2011.3, Condition D
Mechanical Shock	MIL-883B, Method 2002, Condition B: 1,500G for 0.5 ms
Variable Frequency	MIL-883, Method 2007, Condition A: 20-2,000 Hz for 4 mins.; peak at 20 G's.
Thermal Shock	MIL-883, Method 1011.3, Condition B: −55°C to 125°C, 15 cycles
Moisture Resistance	MIL-883B, Method D 1004.3
Resistance to Solvent	MIL-883B, Method 2015.1
Solderability	MIL-883B, Method 2003.2
Lead Integrity	MIL-883B, Method 2004.3
Flammability	Needle Flame, IEC 695-2-2

Bubble