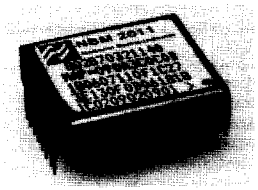
National Semiconductor

November 1980

NBM2011 1M x 1 Magnetic Bubble Memory Device



General Description

The NBM2011 is a 1,048,576 (2^{20}) bit magnetic bubble memory device. All required magnetic components, including the drive field coils, permanent magnets and protective magnetic shield are integral parts of the device. It is packaged in a 1.3 x 1.1 x 0.36 inch 16-pin DIP.

The NBM2011 features a double-period block-replicate organization with true swap gates on the input track. The storage area is arranged as 512 storage loops of 2048 bit locations each. Additional loops are provided for error correction code and defect tolerance. A map of redundant loop data is provided on-chip in one of two dedicated map loops.

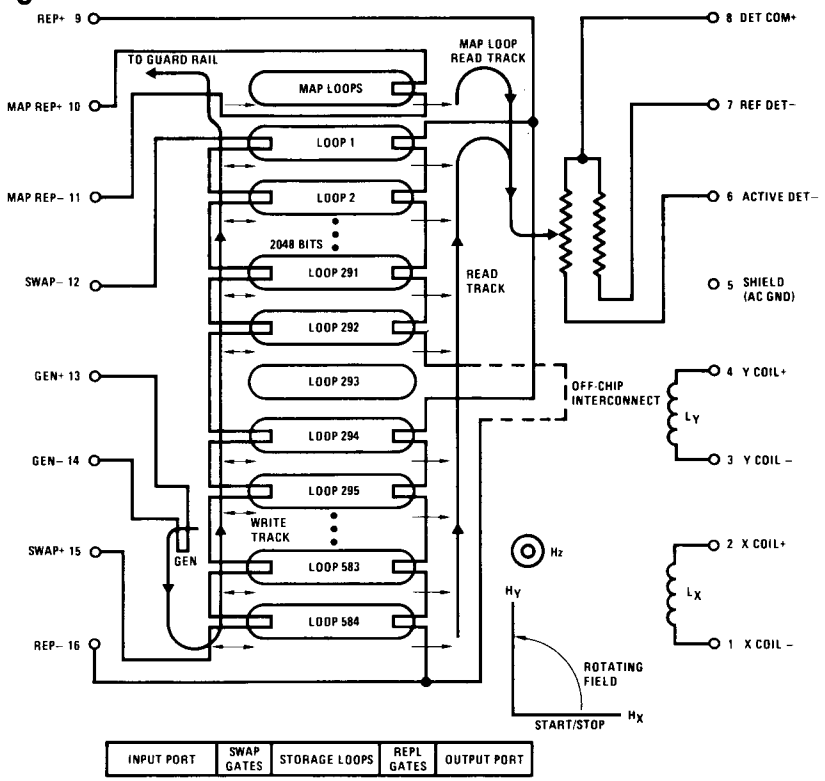
The NBM2011 bubble memory can be operated synchronously or asynchronously. Average access time for a page of data is less than 11.5 ms at 100 kHz. Average power dissipation at 100 kHz is 0.9W. Device performance is guaranteed over a case temperature range of 0°C to 70°C and data is retained without power from −40°C to 100°C.

The device is fabricated using a pseudo-planar process to improve operating margins as well as to enhance reliability. The use of CrCuCr in the conductor elements insures excellent conductivity while greatly enhancing resistance to failure from electromigration.

Features

- Solid state
- Non-volatile
- High density
- Low power
- Page-oriented access
- Start/stop capability
- Modular capacity
- On-chip error map
- Single sense channel required
- Swap gate
- Error correction code storage
- 16 pin dual-in-line package

Chip Organization



IM-FL15M110/Printed in U.S.A.

Absolute Maximum Ratings

Peak Current in X Coil (Subject to Temperature Range Restrictions)	0.9A
Peak Current in Y Coil (Subject to Temperature Range Restrictions)	1.1A
Peak Replicate Current	T.B.D.
Peak Generate Current	T.B.D.
Peak Swap Current	T.B.D.
Peak Detector Current	4.5 mA (Average), 8 mA (Pulse)
Operating Temperature (Case)	0°C to 70°C
Storage Temperature with Data Retention	− 40°C to 100°C
Coil Off Vector Leakage Current Magnitude with Data Retention	10 mA
External Magnetic Field Strength	20 Oe
Maximum Coil Pin Voltage Relative to Any Other Pin	± 40V

Organizational Specifications

Bits/Loop	2048
Total Data Loops	584
Usable Data Loops	524
Error Correction Code Loops	12
User Data Loops	512
Total User Storage	1,048,576 (1M) Bits
Map Loops	2

Recommended Operating Conditions

	Min	Typ	Max	Units
Operating Temperature (Case) (T_C)	0		70	°C
Operating Frequency (f_o)		100		kHz
I/O Data Rate		1		Bit/ Cycle

DC Electrical Characteristics

$T_C = 0°C$ to $70°C$, $f_o = 100$ kHz, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FUNCTION CURRENTS						
I_G	Generate Current		125	150	175	mA
I_S	Swap Current		14	18	22	mA
I_{RC}	Replicate Cut Current		115	125	140	mA
I_{RT}	Replicate Transfer Current		32	40	48	mA
I_{RCM}	Map Replicate Cut Current		57	63	70	mA
I_{RTM}	Map Replicate Transfer Current		16	20	24	mA
I_{DA}, I_{DR}	Detector Current	Active or Reference		4		mA
I_{TM}	Map Loop Transfer Current		− 14	− 18	− 22	mA
COIL						
V_X, V_Y	Coil Driver Supply Voltage	$f_o = 100$ kHz	11.4	12.0	12.6	V
V_{SWITCH}	Coil Driver Switch Drop	2 Switches in Series	0	1.0	1.8	V
V_{CLAMP}	Coil Driver Clamp Diode Drop	2 Diodes in Series	0	2.0	2.7	V
I_{XP}	X Coil Peak Current			630		mA
I_{YP}	Y Coil Peak Current			750		mA
$I_{X\,(offset)}$ $I_{Y\,(offset)}$	Coil Current Offset		− 35		35	mA
$I_{X\,(undershoot)}$	Stop Current Undershoot				10	mA
$t_{S/S}$	Stop/Start Time		− 20	0	20	Degrees
P_c	Allowable Total Coil Power				1.5	W
DEVICE COMPONENT RESISTANCE						
r_G	Generate	0°C 25°C 70°C	4.5 5		 9 11	Ω Ω Ω
r_R	Replicate	0°C 25°C 70°C	110 120		 160 180	Ω Ω Ω
r_S	Swap	0°C 25°C 70°C	550 600		 1000 1200	Ω Ω Ω
r_{RM}	Map Replicate (Including Swap)	0°C 25°C 70°C	27 30		 50 60	Ω Ω Ω
r_{DA}, r_{DR}	Detector (Active and Reference)	0°C 25°C 70°C	900 980		 1500 1800	Ω Ω Ω
r_{DA}/r_{DR}	Detector Resistance Ratio		0.985		1.015	

DC Electrical Characteristics (Continued) $T_C = 0°C$ to $70°C$, $f_o = 100$ kHz, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVE COIL IMPEDANCES						
L_X	X Coil Inductance		45		47	μH
L_Y	Y Coil Inductance		37		40	μH
r_X	X Coil DC Resistance	Non-Operating 25°C	3.4		4.0	Ω
r_Y	Y Coil DC Resistance	Non-Operating 25°C	1.5		1.9	Ω
Z_X	X Coil AC Resistance	0°C Unpowered 70°C Powered	3.3 4.1		3.9 5.3	Ω Ω
Z_Y	Y Coil AC Resistance	0°C Unpowered 70°C Powered	1.6 2.0		2.0 2.7	Ω Ω
OUTPUT SIGNALS						
	Differential AC Peak-to-Peak Output Voltage	4 mA Detector Current				
V_{OH}	Logic 1	Bubble Present	8			mV
V_{OL}	Logic 0	No Bubble			1.5	mV
ΔV_{CM}	Common-Mode Output Signal				50	mV
ΔV_{NC}	Differential Noise Voltage Coupled from Coils	Phase = 190°-245°			1.0	mV

AC Electrical Characteristics (over the operating range)

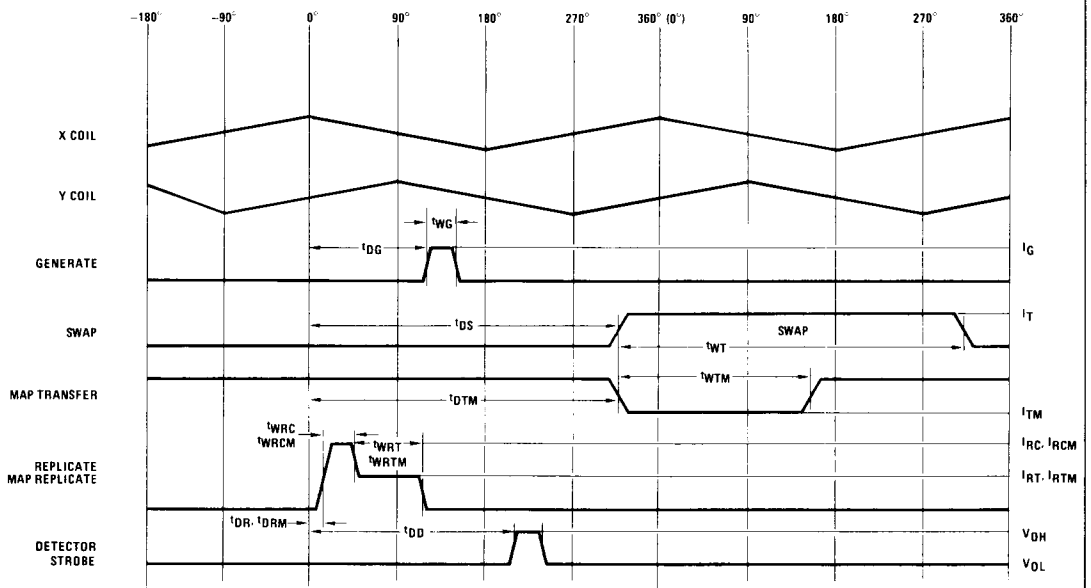
Symbol	Parameter	Conditions	Min	Typ	Max	Units
WRITE CYCLE TIMING						
t_{PGS} (1)	Generate First Bit to Swap In			597		Cycles
t_{PGS} (584)	Generate Last Bit to Swap In			14		Cycles
t_{PSR}	Swap In to Replicate Out			1026		Cycles
t_{PS}	Swap In to Non-Volatile Storage			1		Cycles
t_{DG}	Generate Delay Time		45		150	Degrees
t_{WG}	Generate Pulse Width		83	150	200	ns
t_{DS}	Swap Delay Time		270		330	Degrees
t_{WS}	Swap Pulse Width		340	370	400	Degrees
READ CYCLE TIMING						
t_{PRD}(1)	Replicate Out to Detect First Bit			91		Cycles
t_{PRD}(584)	Replicate Out to Detect Last Bit			674		Cycles
t_{PRS}	Replicate Out to Swap In			1022		Cycles
t_{DR}	Replicate Delay Time		−10		20	Degrees
t_{WRC}	Replicate Cut Pulse Width		T.B.D.	100	T.B.D.	ns
t_{WRT}	Replicate Transfer Pulse Width		80	100	120	Degrees
t_{DD}	Detect Delay Time		190	195	200	Degrees

AC Electrical Characteristics (Continued) (over the operating range)

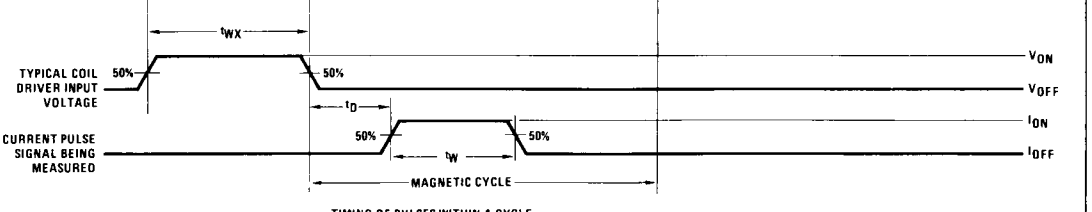
Symbol	Parameter	Conditions	Min	Typ	Max	Units
MAP READ AND WRITE CYCLE TIMING						
t_{PMRD}	Map Replicate to Detect			97		Cycles
t_{SMR}	Map Replicate Set-Up		2			Cycles
t_{PGT1}	Generate to Map Loop #1 Transfer			608		Cycles
t_{PGT2}	Generate to Map Loop #2 Transfer			605		Cycles
t_{ST}	Map Transfer Set-Up		2			Cycles
t_{PTR}	Map Loop Transfer-In to Replicate			1028		Cycles
t_{DRM}	Map Replicate Delay Time		−10		20	Degrees
t_{WRCM}	Map Replicate Cut Pulse Width		T.B.D.	100	T.B.D.	ns
t_{WRTM}	Map Replicate Transfer Pulse Width		80	100	120	Degrees
t_{DTM}	Map Transfer Delay Time		270		330	Degrees
t_{WTM}	Map Transfer Pulse Width		200		240	Degrees

Note: Propagation times are defined from the beginning of the cycle in which the first signal occurs to the beginning of the cycle in which the second signal occurs. Propagation times in cycles listed as typical are exact.

Current Phase Requirements



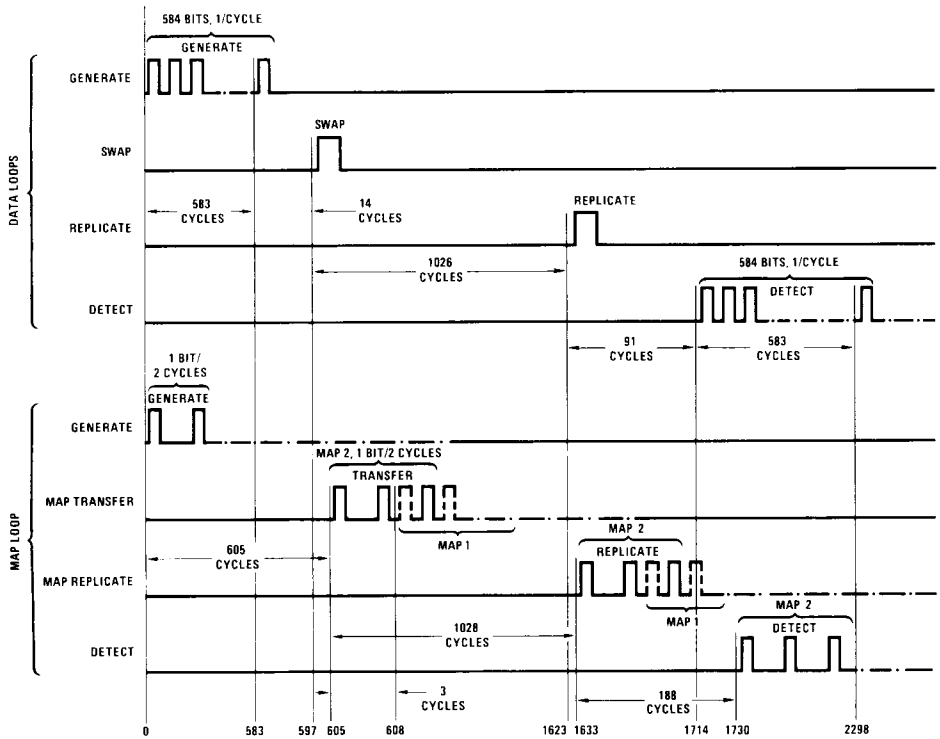
Timing Measurements



TIMING OF PULSES WITHIN A CYCLE

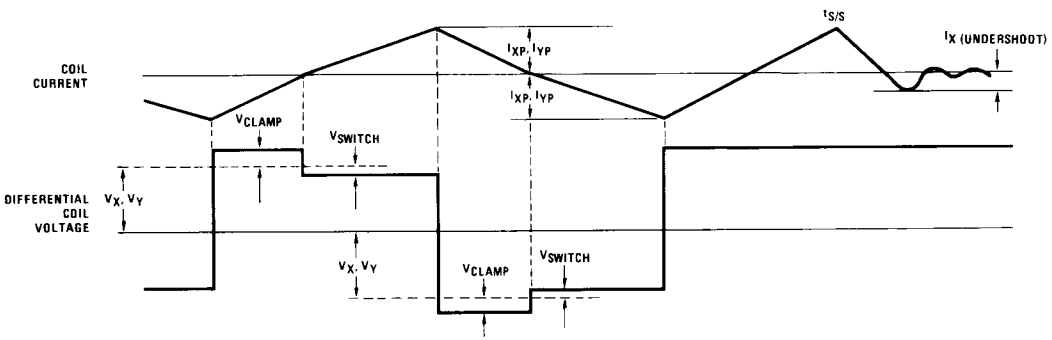
AC Electrical Characteristics (Continued) (over the operating range)

Control Timing



Operating Characteristics

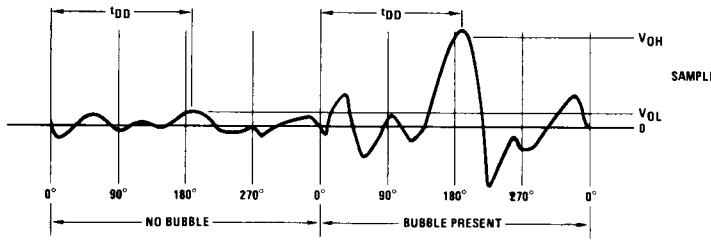
Typical Coil Waveform Imbalance Due to Driver Circuit



Maximum instantaneous vector rotational velocity 4×10^5 radians/sec.

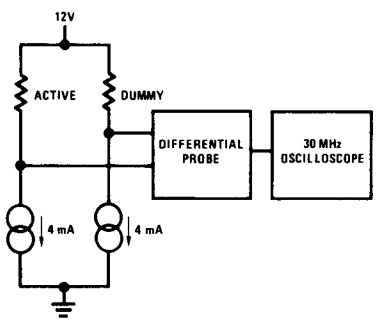
Operating Characteristics (Continued)

Output Signal Timing



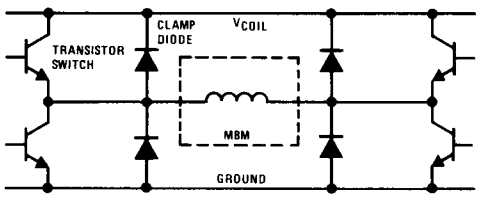
Test Set-Up

Output Detection



Scope input impedance should be < 2 MΩ and > 5 pF
Common-mode rejection < 60 dB frequency response > 30 MHz

Typical Driver Circuit



Device Organization

The NBM2011 features a double-period block-replicate structure. There are a total of 584 minor (data storage) loops containing 2048 positions each. To read from the device, an entire block of data, one bit from each loop, is replicated simultaneously onto the output tracks.

Output

Due to the double-period input and output tracks, the spacing between minor loops is one bit. Hence, upon replication, a consecutive-bit data stream propagates through the detector at a data rate equal to the single-bit shift rate.

Input

One generator feeds the double-period input track. Storage loops align with consecutive positions on the input track. Swap gates on the input track transfer the new bubbles into the storage area and simultaneously transfer the old bubbles out. The use of the swap gates reduces the write cycle time for a single page, as the clearing of the old page is not necessary before writing. It also eliminates the requirement of holding power on for a duration longer than the swap operation in the event of a power failure during a write cycle.

Device Organization (Continued)

Redundancy

Not all of the 584 storage loops are provided for user data storage. 512 loops are available to store data, giving the device a usable capacity of 1,048,576 (1M) bits. Twelve (12) other loops are provided for an error correction code. The remaining 60 loops are defined as redundant.

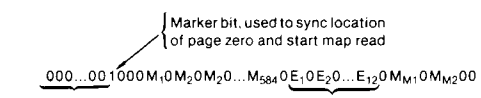
Redundancy is utilized in magnetic bubble technology to improve yield. Sixty (60) loops are declared redundant; these consist of any defective loops and a balance of arbitrary good loops. Redundant loops are mapped out by the user's control circuitry.

Redundancy Map

Two (2) map loops are provided in addition to the 584 storage loops. These loops have their own transfer-in and replicate gates but use the same generator and detector as the storage loops. One of the redundancy map loops is loaded with the redundancy information identifying which storage loops are usable. A "one" designates a usable loop; a "zero" indicates a non-usable loop. Preceding this map code is a stream of 64 "zeros" followed by "one" which can be used to synchronize the external control circuitry with the memory. The redundancy map loop used for storage of the map is also identified in the code (see Coding of Redundancy Map Loop). Since only alternate bit positions are written in the map loop (for improved reliability), every other bit is always zero.

The redundancy map is also printed onto two labels on each device using a hexadecimal format. A ">" at the end of the last line on the top label indicates that the map is continued on the bottom (underside of device) label.Two digits are used per loop but instead of providing the absolute loop number the incremental difference between the non-usable loops is printed. For example, if the first bad loop is loop #7, a "06" is printed and if the next two bad loops are 19 and 23, a "0C" will be followed by a "04". This allows the use of two hexadecimal digits for an incremental difference between two bad loops of up to 256 (FF).

Coding of Redundancy Map Loop



M_i = Map bit for loop i

M_{M1} = Map bit for map loop 1

1 = good loop

0 = bad loop

Note: Loop 283 is not connected on the NBM2011, yielding a total of 584 – 1 = 583 potentially good loops.

Functional Description

Write Operation

Writing data is accomplished by generating the new data with a series of pulses applied to pins 13 and 14, starting $t_{PGS}(1)$ before the swap operation. As the device continues to cycle after all data is generated, the new data and the old will be aligned at the swap gates after t_{PGS} (584). A swap pulse is applied to pins 12 and 16 at this time, swapping the new data in and the old data out. Old data are propagated out and discarded beyond the guard rail.

Read Data Operation

To read data, the device must be cycled until the desired page is aligned with the replicate gates on the output side of the storage loops. A replicate cut pulse is applied to pins 9 and 16 to duplicate the page. This is immediately followed by a replicate transfer pulse which causes the duplicate bubbles to propagate into consecutive positions on the output track.

Propagation along the output tracks occurs during t_{PRD}. Detection occurs when a bubble passes under the magnetoresistive detector element. The bubble's magnetic field causes the detector element to change resistance. By passing a constant current through the detector, this is converted to a voltage signal. A dummy detector which is not influenced by magnetic bubbles is used to cancel the background magnetoresistive signal.

Output bubbles are discarded beyond the guard rail after detection. A complete page is read in t_{PRD} (584).

Map Read Operation

To read the contents of the map, a series of alternate cycle replicate pulses, identical to data replicate pulses, is applied to pins 10 and 11. Data will be available after t_{PMRD}. Since map data is only loaded into alternate positions in one loop, one pass may result in no data. This will require repeating this procedure after delaying one cycle. See "Coding of Redundancy Map Loops" for decoding information.

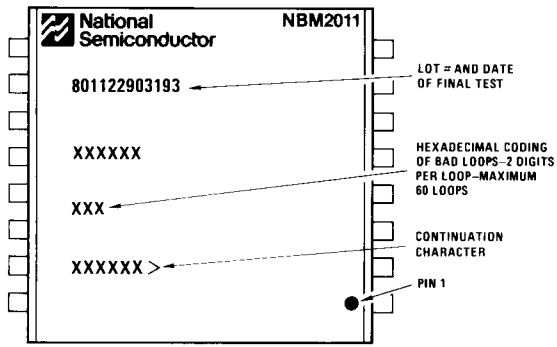
Map Write Operation

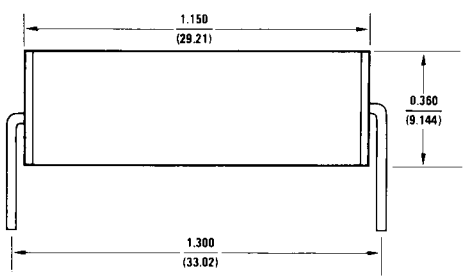
Writing the map loop is accomplished by generating map information as normal data. After t_{PGT1} or t_{PGT2}, pins 10 and 11 are pulsed with a series of negative map transfer pulses on alternate cycles. Selecting t_{PGT1} writes into map loop 1; selecting t_{PGT2} writes into map loop 2. Since the loading of the map loops is normally done at the factory during final test, the system designer does not need the negative polarity driver.

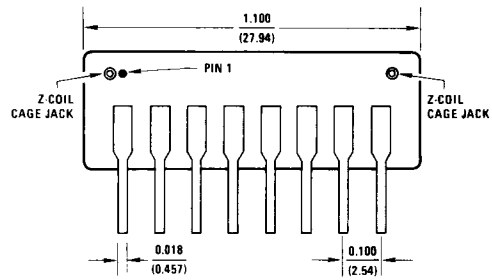
Physical Dimensions inches (millimeters)

Mechanical Data

The NBM2011 is packaged in a 16-pin dual-in-line package. The die is mounted on a PC carrier which is attached to the beryllium copper lead frame and encapsulated in electrically non-conductive plastic compound. The package also contains two orthogonal coils along with barium ferrite permanent magnets with spreader plates. The outer casing of the package is made from MU-metal which acts as a magnetic shield. A Z-coil of 17 3/4 turns is included in the package and is used during factory testing. The package weighs approximately 28 grams.







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